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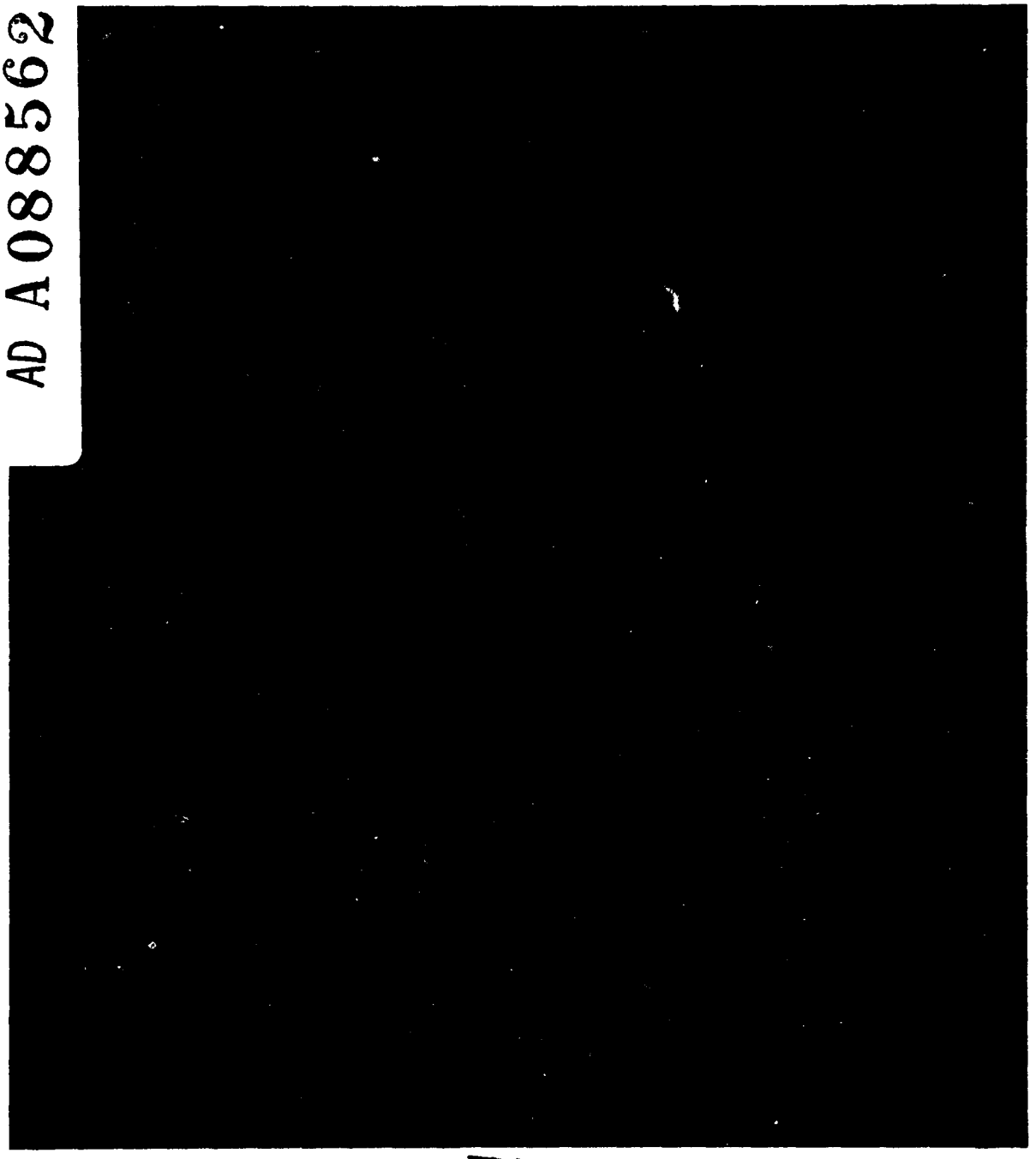

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This is the third semiannual report of a program to demonstrate that low temperature processing techniques, particularly pulsed electron beam surface heating, can eliminate the need for high temperature thermal cycling of silicon wafers in fabricating very large scale integrated (VLSI) devices. This report describes results using pulsed annealing techniques to fabricate: (1) low leakage diodes, (2) ion-implanted resistors defined by thin (2.5 micron) oxide windows, and (3) small geometry patterns to

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measure lateral diffusion of dopants. Comparison to high temperature thermal processing was favorable.

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SUMMARY

The objective of this program is to demonstrate that the maximum temperature used in thermal processing of silicon integrated circuits can be reduced by the use of large area pulsed electron beams. Maintaining lower temperatures during fabrication will reduce plastic deformation and distortion of the substrate, reduce unwanted diffusion from buried layers, reduce the formation of defects, precipitates, etc., and in general, increase the yield for very small line widths.

The specific processes studied in this program are the formation of epitaxial silicon on silicon layers, and annealing of ion implantation damage. Both processes now require temperatures in excess of 900°C (typical). Results to date indicate that the use of a pulsed electron beam (PEB) to replace high temperature cycles allows the reduction of processing temperatures to 600°C or lower. Specifically, it has been demonstrated that:

- Polysilicon films deposited at 600°C by LPCVD can be regrown, epitaxially, to a single crystal by PEB processing.
- Arsenic, boron, and phosphorus ion implants in the energy range 0-100keV and for dose levels 10^{13} - 10^{16} ions/cm^2 can be annealed by PEB processing.
- Devices (diodes, transistors) with good electrical characteristics can be formed by PEB processing.
- Oxide masks can be used to define PEB processing areas to better than 2 micron resolution.

The demonstration that lateral resolution of PEB processing is below one micron (for VLSI structures) is an objective of the last six months of this program.

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SECTION 1
INTRODUCTION

1.1 PROGRAM OBJECTIVES

The goal of this program is to reduce the maximum temperature used in processing large scale integrated circuits by using large area pulsed electron beams. Specifically, the program is to demonstrate: (1) that a thin silicon film can be deposited at low temperatures with impurity levels consistent with requirements for submicron devices, (2) that the structure of this film can be changed from amorphous or polycrystalline to single crystal through pulsed irradiation by electron beams, (3) that ion implanted junctions can be annealed by pulsed technology, and (4) that an operational device typical of very large scale integrated (VLSI) technologies can be fabricated by these techniques.

1.2 TECHNICAL CONSIDERATIONS

Existing technology for the fabrication of integrated circuits uses high temperatures (over 1000°C) for the growth of epitaxial films[1] and annealing of ion implantation damage[2]. Plastic deformation of the substrate and diffusion from previously deposited layers occurs at these temperatures, but the effect is not limiting until devices employ submicron dimensions[3]. This program is to demonstrate that epitaxial films can be formed at low temperatures, that active device junctions formed by ion implantation can be annealed without heating the substrate to high temperatures, and that the motion of dopants in both processes is restricted.

1.3 GENERAL METHODS

High temperature furnace processing steps are replaced by pulsed electron beam surface heating[4]. Through control of beam fluence and particle energy this electron beam can be used to heat (or melt) up to 1.0 micron of silicon, heating the bulk of the substrate no more than 10°C. Short period thermal gradients cause epitaxial crystal regrowth in the heated surface material to anneal ion implantation damage and recrystallize deposited films. Combined with a low temperature deposition technique to put down an appropriate film, the technique described can form a lightly doped high quality epitaxial film over a heavily doped substrate. To anneal ion implanted junctions

for small scale active devices, a process has been developed based upon a multiple step, low temperature furnace and low fluence pulsed electron beam treatment.

1.4 TECHNICAL RESULTS/CONCLUSIONS

This program has:

- Identified an optimum low temperature film deposition process.
- Demonstrated pulsed electron beam epitaxial regrowth of this deposited film.
- Demonstrated pulsed electron beam annealing (PEBA) of varying dose ion implanted junctions.

During the past six months this program has:

- Used PEBA to fabricate low leakage diodes.
- Used PEBA to fabricate bipolar transistors.
- Demonstrated that thin oxide layers can be used to mask PEBA.
- Demonstrated 2 micron linewidth resolution with PEBA, improvements predicted.

During the past six months emphasis was placed on the fabrication (and testing) of simple device structures using pulsed electron beam annealing (PEBA) of ion implantation damage as the key low temperature processing step. It has been demonstrated that this process can be used to fabricate typical LSI structures, with future work aimed at showing applicability to smaller geometries. Diodes, implanted resistors, and bipolar transistors were completed and tested. Field effect transistor (FET) structures are in process.

The electrical measurements were restricted to high current and low current I-V curves. The diodes fashioned with oxide defined structures showed low leakage currents, low diffusion currents, and low series resistance with results comparable to thermal anneal cycles. The bipolar transistors which were pulse annealed had a gain of 40 and were also comparable to identical but thermally annealed devices. Ion implanted resistors were used to test pulse annealing of low dose implants. In these

experiments activation of the dopant by PEBA was better than that achieved in a low temperature anneal cycle by a factor of two to three. Also, these ion implanted, PEBA resistors showed no variation in sheet resistance for changes in oxide window width from 2 to 50 microns. Additional electrical measurements, including C-V profiles and measurement of carrier lifetime and diffusion length, are in progress.

Additional equipment was added to the pulsed electron beam processor which enables us to raise the sample temperature to over 400°C during the short pulse. Preliminary results, based upon photovoltaic voltage measurements, indicate that pulsing heated samples (400°C) prevents the quenching-in of point defects. Heating a sample to 400°C for 10 minutes after pulse processing cold (20°C) is sufficient to anneal most of the defects attributed to quenching. However, pulse processing a heated sample appears better.

1.5 FUTURE DIRECTIONS

During the last six months of this program, the principal effort will again be placed on electrical characterization of pulsed electron beam processed junctions and on geometrical effects related to VLSI structures. The latter refers to submicron gate widths in FET structures. Two related experiments are planned: (1) measurement of the lateral diffusion of a junction under an oxide film (to 0.1 micron resolution) which was fabricated by ion implantation and PEBA and (2) measurement of the uniformity of processing by PEBA to 1-2 micron resolution. Planned experiments on electrical characterization include DLTS (delay-line transient spectroscopy) for PEBA diodes, and I-V curves for JFETs formed by PEBA in conventional CVD epitaxial layers and in pulsed epitaxial layers. Additional experiments to determine the limitations on pulsed solid phase annealing will be performed.

SECTION 2
TECHNICAL INFORMATION

2.1 OBJECTIVES

To fulfill the goals of this program, the past six months were devoted to the fabrication and testing of simple device structures to measure the electrical properties of pulse processed material, and to assess geometrical properties of the process. The specific experiments planned were:

1) Fabricate low leakage current diodes to compare PEBA and thermal annealing cycles.
2) Test PEBA of low dose, ion implanted junctions (about 10^{12}-10^{13} ions/cm^2) where a second implant is required for adequate ohmic contact.
3) Test the effect of PEBA on oxide defined structures with typical LSI scales.
4) Measure lateral diffusion of dopants after pulse annealing.
5) Determine the effect of PEBA on two overlapping ion-implants of different junction depths (bipolar transistors).
6) Fabricate JFET structure in pulse epitaxy material using PEBA for junctions.
7) Determine the effect of varying sample temperature during pulse annealing.

These experiments, described in sections 2.2 through 2.6, were all successful. The JFET structure, however, is still in process due to a greater number of fabrication steps.

2.2 DIODES

In previous experiments, diodes were fabricated by ion-implantation of the entire surface of a two-inch silicon wafer, followed by different annealing procedures, mesa etching, and the application of contacts. Most measurements were made on the whole wafer before etching. The mesa etched diodes were found to be leaky, and low current I-V measurements were not felt to be worthwhile to compare thermal and pulse annealing processes.

To reduce leakage currents, ion implants were first tried as isolation after annealing the whole surface of a wafer. When this, too, failed a mask set was made up for diodes defined by etched oxides. This structure, shown in Figure 1, worked well for

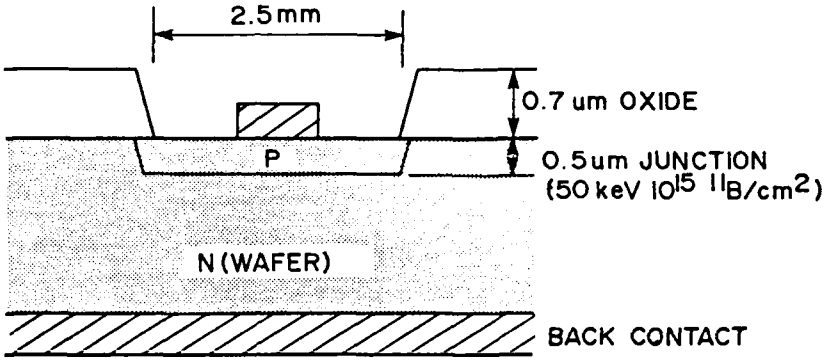


Figure 1. Structure of p^+ on n diodes

low temperature annealing of p implants into n-type material. For high temperature anneal steps, or for diodes of the reverse order, n implanted into p-type material, the lack of a guard ring created poor devices. A different mask set (section 3.2) will be used for future tests with silicon diodes.

The complete matrix for the p on n diodes shown in Figure 1 is given in Table 1. For different junction depths, or ion implant energies, PEBA was compared to low and high temperature furnace anneal cycles. Two irradiation levels were selected for the pulse process, corresponding to a fluence above that required to melt the surface of a crystalline (c-Si) silicon wafer (1 joule/cm^2), or to a fluence below that required to melt a thin amorphous (a-Si) surfical layer (0.6 joule/cm^2)[5]. Thus melting and nonmelting pulse anneals were tested.

TABLE 1. PROCESS MATRIX FOR 100 mil P^+ ON N DIODES

Ion Implant Energy (keV) (10^{15} $^{11}B^+/cm^2$)	Annealing Cycle 550°C, 1 hour plus (shown), followed by 550°C, 1 hour
25	none
50	950°C, 15 minutes
100	PEBA at 0.6 J/cm^2
200	PEBA at 1.0 J/cm^2

After annealing, contacts (Ti-Pd-Ag) were applied and sintered. The devices were then tested without dicing the wafer. High current I-V characteristics were measured for five to twenty devices on each wafer using a curve tracer. Typical results are shown in Figures 2 and 3. Low current I-V response, in the dark, was measured for the two best devices on each wafer. Results for the 50 keV implant series are shown in Figures 4 and 5. Extrapolated values from Figure 5 for the diode response curve $J = J_o (\exp (qV/mkT) - 1)$, are given in Table 2.

TABLE 2. DIODE CHARACTERISTICS FROM FIGURE 5
($J = J_o \exp (qV/mkT-1)$)

Anneal Cycle	Ideality Factor, m	Diffusion Current, J_o (A/cm^2)
550°C, 2 hr	1.08	6.5×10^{-10}
550°C, 1 hr + PEBA at 0.6 J/cm^2 + 550°C, 1 hr	1.09	2.8×10^{-10}
550°C, 1 hr + PEBA at 1.0 J/cm^2 + 550°C, 1 hr	1.14	6.8×10^{-10}

Summarizing the results, all low temperature annealed devices (550°C only) had low leakage currents and diffusion currents, but high series resistance. This is expected as the low temperature anneal would not activate a high percentage of the implanted dopant. All of the high temperature (950°C) annealed devices showed very high leakage and diffusion currents. It is believed that the resist was not completely stripped after ion implantation, and that contaminants were driven to the oxide-silicon interface during the high temperature anneal. Similarly, all high fluence PEBA samples showed increased leakage currents, which might also be attributed to contamination. However, as this pulse process did not melt the entire oxide layer, or the silicon below it, contaminants were restricted and leakage currents were better than from the furnace anneal. The low fluence PEBA process was very successful on all implants except the 200 keV case. Leakage and diffusion currents were similar to the low temperature thermal anneal, whereas the series resistance dropped by more than a factor of four.

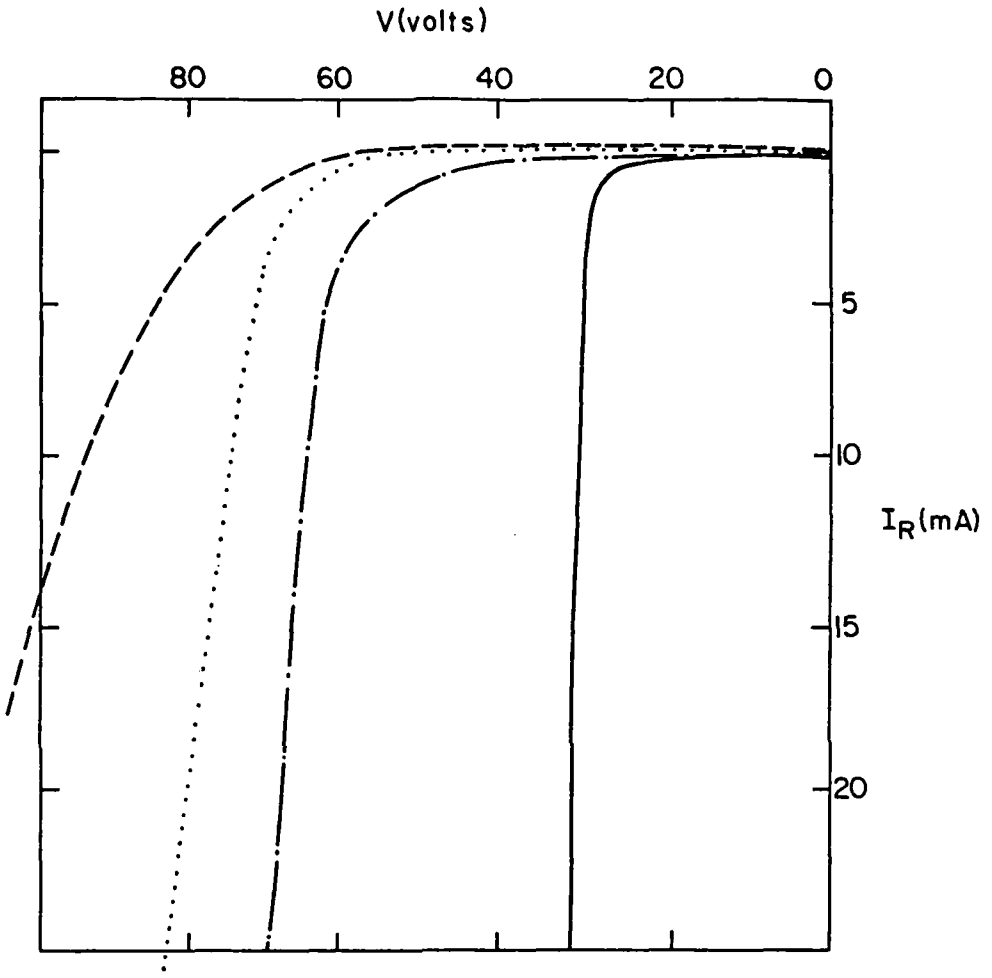


Figure 2. Reverse current I-V curves for p^+ on n diodes showing greater breakdown voltage for low temperature and low fluence PEBA anneals.

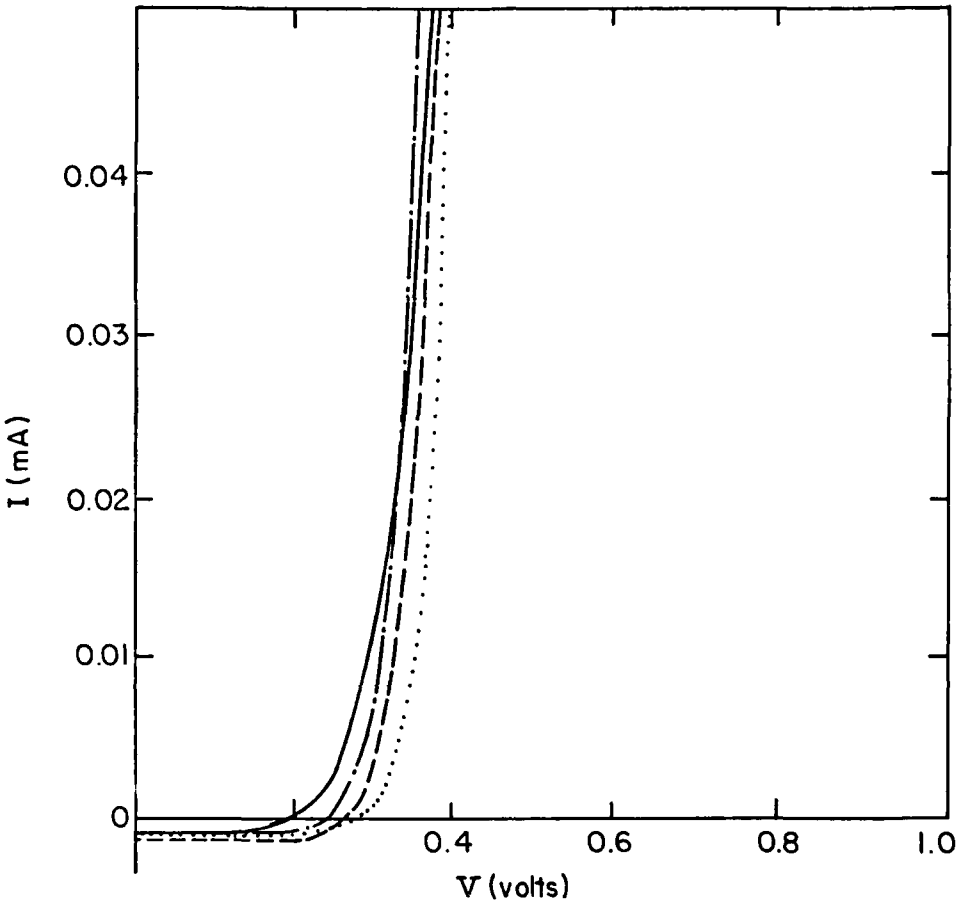


Figure 3. Forward current I-V curve for p^+ on n diodes, linear scales.

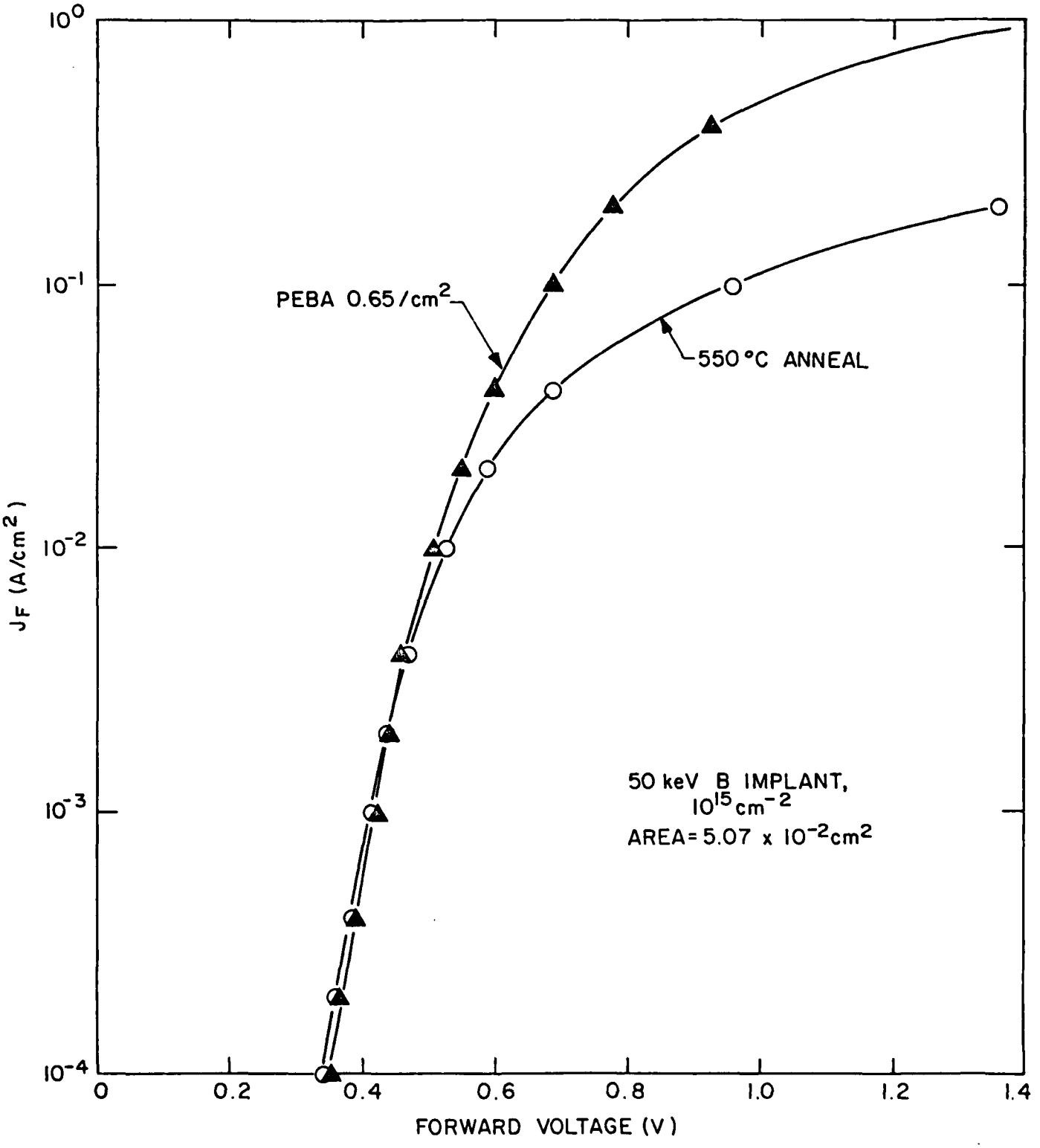


Figure 4. Forward current I-V curve for p^+ on n diode, logarithmic scale, showing PEBA diode had series resistance factor of 4 lower than 550°C (only) anneal.

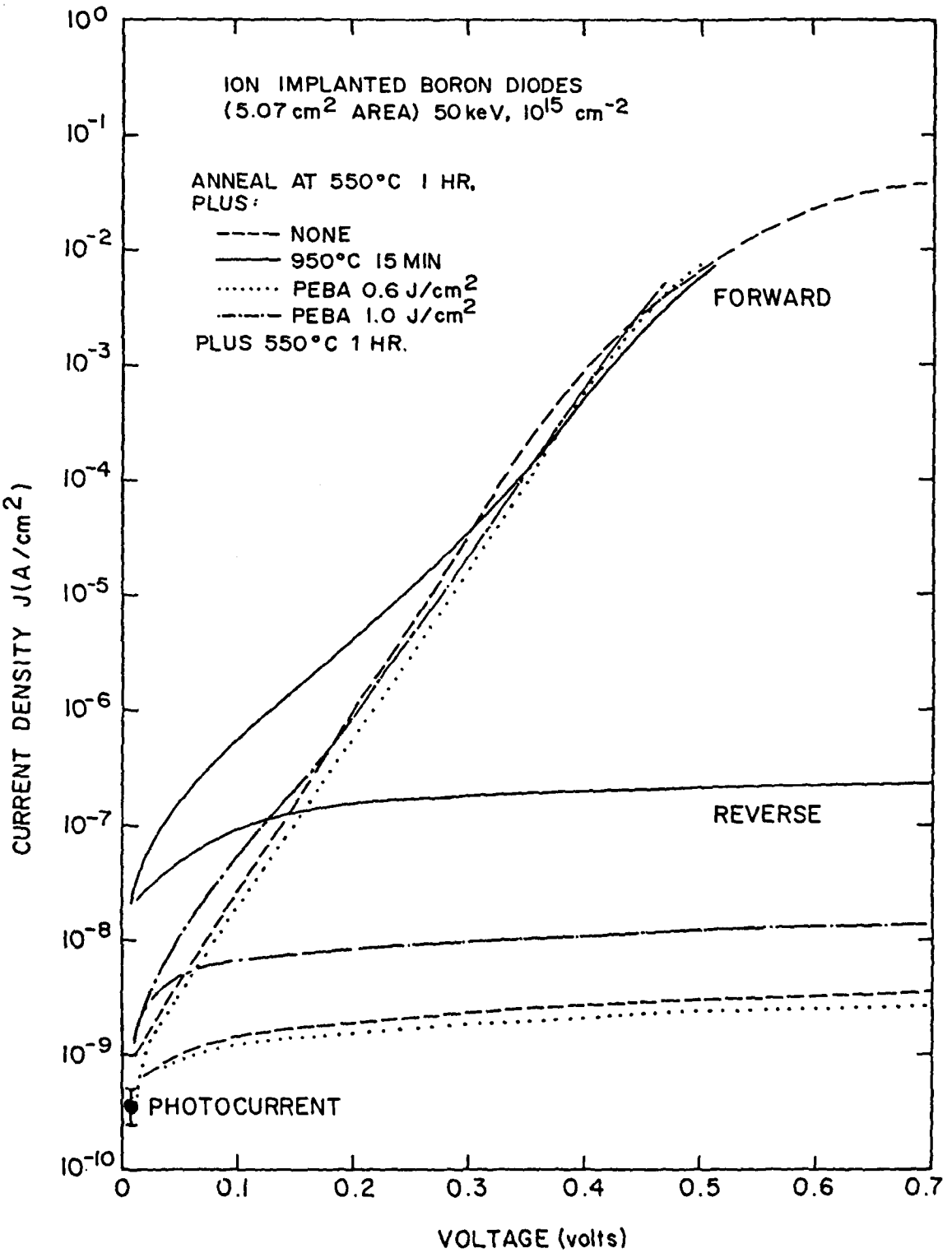


Figure 5. Low current I-V curve for p^+ on n diode, logarithmic scale, showing low leakage currents for low fluence PEBA processed diode.

The conclusion is that the low temperature anneal results in lattice regrowth, whereas the pulse (nonmelting) anneal serves to activate more of the implanted dopant. The junction formed by boron implanted at 200 keV was just too deep to be significantly affected by the low fluence, low energy electron beam.

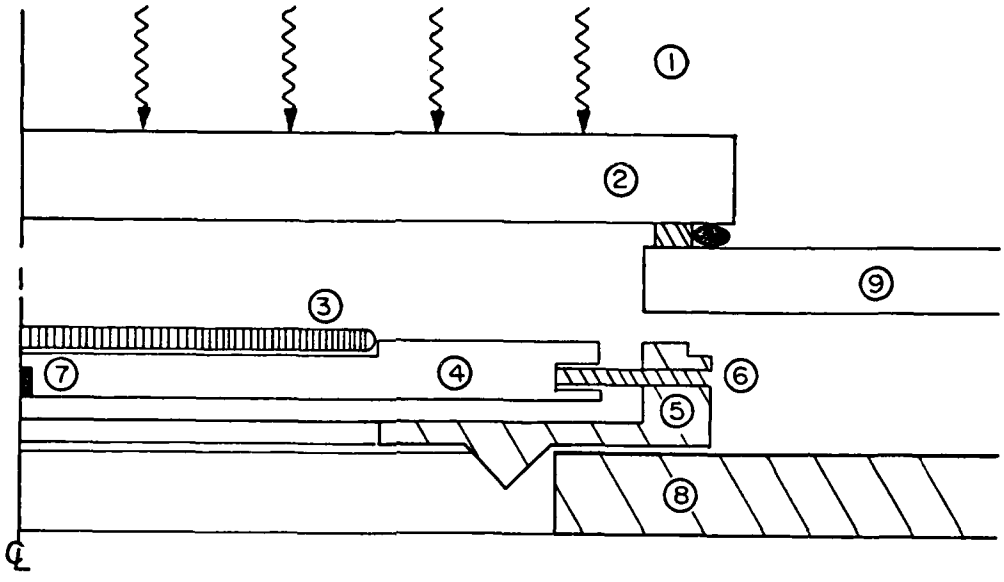
2.3 SAMPLE TEMPERATURE EFFECTS

All samples pulse heated during this program were held at room temperature during processing. The sample temperature typically increased by less than $2^{o}C$ as a result of pulse processing. The effects of heating a wafer, while pulsing, to a temperature of about $400^{o}C$ would be:

- to reduce the fluence required to melt the sample surface, or to increase the melt depth at a fixed fluence.
- to reduce thermal gradients, which would relieve thermally induced stresses and reduce the velocity of the liquid-solid interface during epitaxial crystal regrowth.
- to reduce point defect concentration caused by fast quenching of the surface.

Heating of a sample to moderate temperatures would appear to be beneficial except that more complex apparatus is required for processing.

To test this possibility, the apparatus shown in Figure 6 was constructed to heat a sample wafer up to $400^{o}C$ in vacuum just before pulsing with an electron beam. This apparatus is designed so as not to change any parameters of the normal pulse processing. The heating element is an infrared lamp, mounted outside the vacuum chamber and focused onto the sample through a transparent window. The sample is mounted on a thermally isolated, electrically grounded carbon disk. A thermocouple is fixed to the underside of the disk. The carbon disk also serves as a mount for small samples and increases the heat capacity of the isolated system. The increase in heat capacity is sufficient to reduce the cooling rate, after removing the heat source, to less than $1^{o}C$/sec. After the sample is heated, in typically 10 minutes, it is moved and pulsed in less than 30 seconds, before the sample temperature drops significantly. Better thermal control could have been achieved with a heating element directly beneath the wafer in the vacuum chamber, but then the cathode, anode, and mounting pieces would have been heated too, and the requirement for extra space for the heater would have changed the magnetic field configuration. As constructed, processing parameters remain unchanged.



1. Radiant heat source, outside of vacuum chamber.
2. Glass port, air cooled.
3. Two-inch sample wafer.
4. Carbon disk.
5. Aluminum disk (normal holder assembly)
6. Set-screw thermal isolation (8).
7. Thermocouple (wires not shown).
8. Carousel for transport to diode.
9. Vacuum chamber top.

Figure 6. Schematic diagram of apparatus for pulsing heated wafers. (Note that drawing is double actual scale. Low inductance electrical contact with thermal isolation provided by eight 0-80 setscrews.)

Initial tests with this apparatus were performed on solar cell materials whose parameters have been well characterized at Spire Corporation.[6] Two-inch p-type (1-2 ohm-cm) wafers with an aluminum alloy back contact were implanted with phosphorus at 10 keV to a dose of 2.5×10^{15} ions/cm^2. This is sufficient to turn the surface of the wafers amorphous. Samples were then heated and pulsed. Measurements of sheet resistance (V/I) and point contact photovoltage under AM0 illumination were made immediately; characterization is continuing. The results for different anneal cycles are given in Table 3. The rationale behind the multiple thermal cycles was to separate the effect of preheating or postheating the sample after pulsing, compared to the effect of actually pulsing a hot wafer. A drop in photovoltage (or open-circuit voltage V_{oc}) is an indication of defects near the junction region. The interpretation of the results in Table 2 is that pulsing a cold wafer leaves some "defects" (type unknown) due to thermal quenching, and that most of these defects anneal out in a short time at 400°C. However, pulsing a heated wafer resulted in fewer defects, possibly none, compared to postpulse annealing.

2.4 ION IMPLANTED RESISTORS

This was a test of two important aspects of pulsed electron beam annealing: (1) the annealing of low dose ion implants and (2) annealing through openings in an oxide mask. Previously[6], low dose implants into bare wafers were pulse processed, but adequate measurements could not be made due to the difficulty in contacting the surface region. Instead of trying to recover the previous experimental results, a new test was devised using a mask set to provide defined areas of implantation and contacts. This allowed the accurate measurement of sheet resistance and dopant activation for low dose implants. By varying the size of the opening in the oxide film, geometrical effects of pulsed electron beam annealing could also be determined. Note that the diode characteristics of the low dose, ion implanted junction cannot be separated from the effects of the diode formed by the high dose implant required for ohmic contact.

The geometry of the resistors is shown in Figure 7. The insulating surface oxide was 0.7 micron thick, and the openings (windows) etched in it for resistors were 50, 12.5, 5.0, 2.5, and 1.25 microns wide. Boron, at 25 keV and 100 keV, was implanted into these windows at doses from 10^{12} to 3×10^{14} ions/cm^2. This was followed by a second implant at 3×10^{14} ions/cm^2 into the regions under the contact, as defined by resist. This resist was stripped, and all samples annealed at 550°C for 1 hour prior to pulse processing half of each wafer. Melting anneal parameters (section 2.1) were used. There was no postpulse anneal other than the sinter of contacts at 480°C for 10 minutes.

TABLE 3. EFFECTS OF HEATING SAMPLE DURING PEBA

Thermal Cycle	V/I (ohms)	V_{oc} (mV)
Pulse	4.25	511 - 518
Heat to 400°C in 10 min., cool	61 - 69	475 - 505
Heat to 400°C in 10 min., Pulse at 400°C, cool	3.9 - 4.1	545 - 558
(Repeat, 2nd wafer)	4.1 - 5.3	550 - 555
Pulse, Heat to 400°C in 10 min., cool	4.4 - 5.4	545
(Repeat 2nd wafer)	5.8 - 8.8	543 - 548
Heat to 400°C in 10 min., Pulse at 400°C (30 s) Maintain 400°C for 10 min., cool	4.4 - 5.4	550
Heat to 400°C in 10 min., Cool below 250°C in 5 min., Pulse	4.6 - 5.0	520 - 525
Furnace (in N_2 gas) 550°C 2 hrs, 850°C 15 min, 550°C 2 hrs	10	560

Notes: PEBA fluence 1.0 J/cm^2.
Radiant heating and cooling in vacuum, except for furnace.

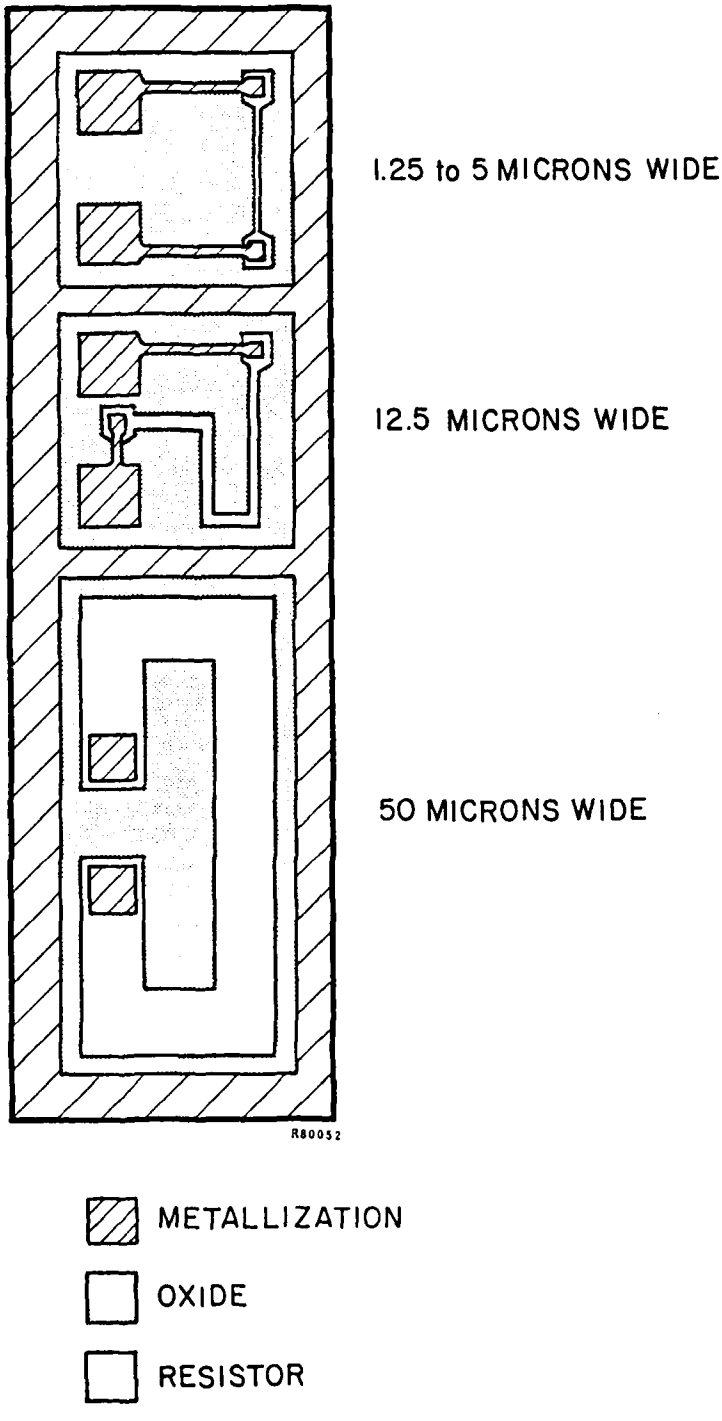


Figure 7. Ion implanted resistor test patterns for analyzing pulsed electron beam annealing (PEBA) with patterned oxides for device structures and with low dose implants.

The results are presented in Table 4, as a function of implant dose. Data are averages from 5 to 10 devices. Testing was difficult without an automated prober. Pulsed electron beam annealing lowered the sheet resistance of low-temperature-only thermal anneals by a factor of 2 to 3. However, the final sheet resistance was still higher than predicted by a factor of 2 to 3. A comparison to a high temperature anneal is in process.

TABLE 4. SHEET RESISTANCE OF ION-IMPLANTED, PULSE ANNEALED 50 MICRON WIDE RESISTORS AS A FUNCTION OF IMPLANT DOSE

		Sheet Resistance ($k\Omega/\square$)		
			Measured Values	
Boron Dose (cm^{-2})	Ion Energy (keV)	Calculated $R_S = (nq\mu)^{-1}$	Pulse Anneal	550°C Only
$1x10^{12}$	25	15.5	∞	28
$3x10^{12}$	100	8.4	12 - 14	—
$1x10^{13}$	25	2.5	6.8	8.5
$1x10^{13}$	100	3.6	4.5 - 5.2	—
$3x10^{13}$	25	1.2	3.6	5.0
$3x10^{13}$	100	1.4	1.5 - 2.6	—
$3x10^{14}$	100	0.21	0.33 - 0.65	—

There was no variation in sheet resistance with window width as shown in Table 5. Some variation in the designed width, from over etching the oxide, was observed for the smallest resistor (1.25 micron), and the corrected data are good. These data imply that lateral diffusion of the implanted dopant during PEBA must be less than 0.25 micron. If diffusion were greater, the sheet resistance of the 2.5 micron window (the smallest accurately defined opening) would vary by more than 20%, which was not observed. Figure 8 shows the effect of this high fluence pulse on a 2.5 micron oxide window at extreme magnification. Despite the fact that the exposed silicon surface was melted, the oxide shows no damage of the reported character[7,8] for samples processed at very high fluence. The PEBA process <u>can</u> be effectively used with oxide masks.

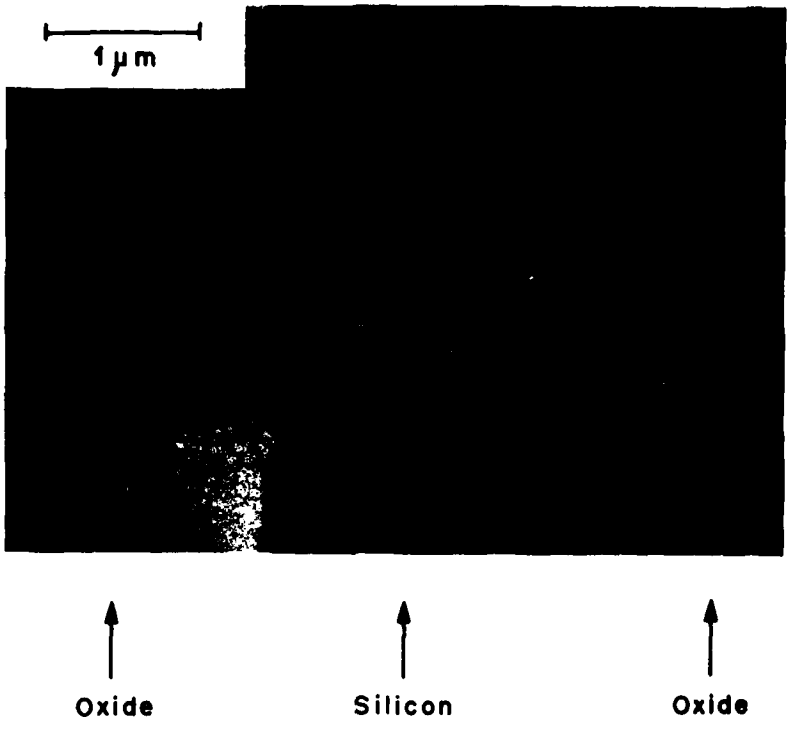


Figure 8. SEM microphotograph of an oxide window (2.5 micron width resistor) showing no damage to interface despite melting of exposed silicon during PEBA.

TABLE 5. SHEET RESISTANCE OF ION-IMPLANTED, PULSE ANNEALED RESISTORS AS A FUNCTION OF RESISTOR (OXIDE WINDOW) WIDTH (25 keV $^{11}B^+$ at $3x10^{13}$ ions/cm^2)

Window Width		Total Area	Sheet Resistance
Microns	Mils	□'s	kΩ/□
50	2	11	3.0
12.5	0.5	23	2.7
5.0	0.2	22	2.75
2.5	0.1	22	2.50
1.25	0.05	22	1.6*

*Resistor width greater than 1.25 microns, area uncertain.

2.5 LATERAL DIFFUSION

The previously described experiment contained an indirect test of lateral diffusion. The measured sheet resistance of an implanted resistor, with a high L/W (length/width) ratio, would change if lateral diffusion affected W; however, the percent activation of dopant, mobility, and other electrical properties will change the sheet resistance too. A simple comparison of R_{SHEET} for different window widths could be misleading.

The test was redefined, using a different pattern, to determine the possible motion of the dopant directly. The repetitive interlocking finger pattern shown in Figure 9 was etched into a 0.7 micron thick oxide film on a 1-2 ohm-cm substrate. This pattern was implanted with 25 keV, $^{75}As^+$ ions to a dose of 10^{15} ions/cm^2. This is sufficient to give dopant concentrations in excess of $10^{20}/cm^3$ in the shallow junction region, a high value chosen for driving the diffusion. After implantation the oxide was removed from half of the samples to check for differences during PEBA where the whole sample surface would be melted, compared to the case where melt was restricted by an oxide mask. Pulse processing was performed at melting and nonmelting fluence. In the low fluence case a 550°C, 1 hour thermal cycle preceded PEBA.

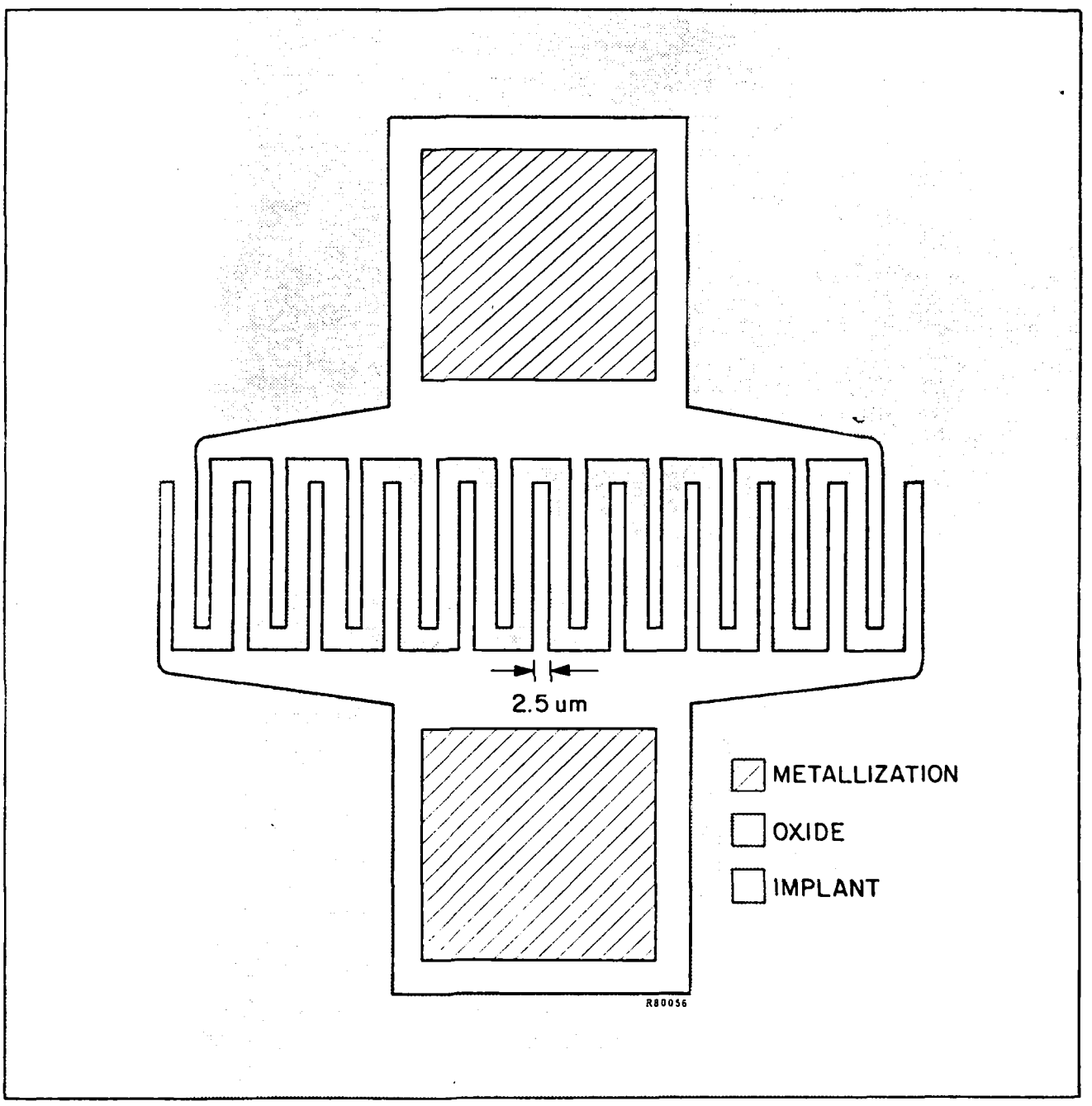


Figure 9. Parallel line structure used to investigate lateral dopant motion during pulsed electron beam annealing.

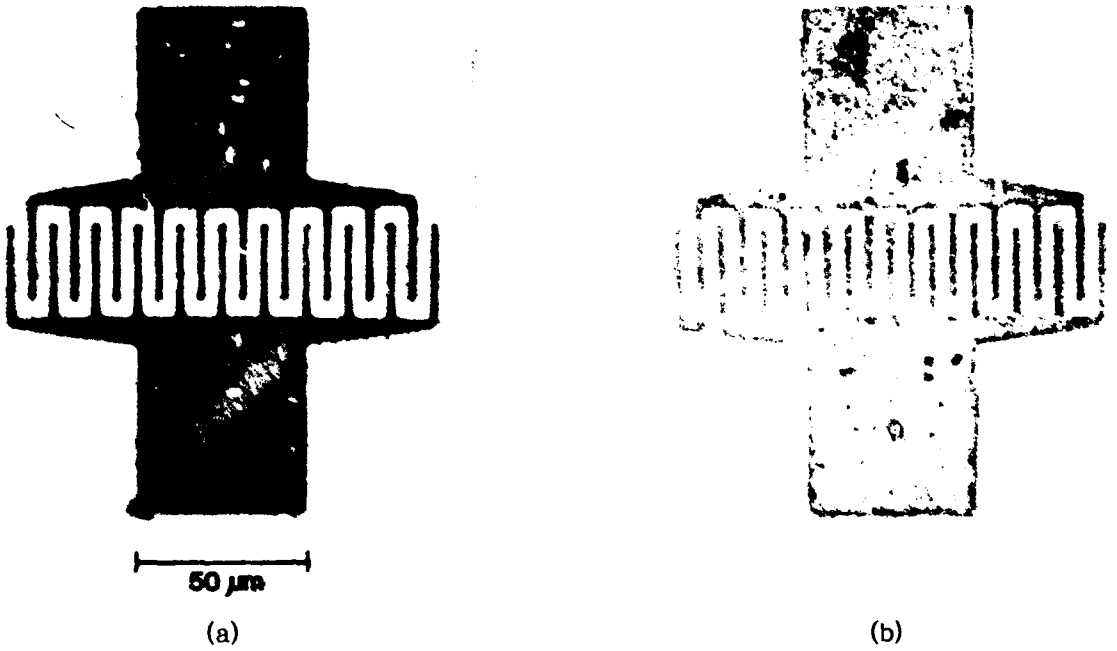


Figure 10. Stained surface patterns (n^+ regions) of pattern in Figure 10: (a) as implanted and (b) after removing oxide and PEBA at 1.2 J/cm^2. (Note that lateral motion of dopant in worst case tested was less than 0.5 micron.)

The results are shown in Figure 10. A stain for the n^+ region was used after cleaning the surface and removing any oxide (if present). Figure 10(a) shows the stain for an implanted, unannealed region. Although most of the implanted arsenic was not substitutional, the stain did attack the implanted region and good resolution was obtained. The effects of annealing under different conditions did not change this pattern significantly. The principal error in the measurement was random variation in the width of the etched oxide patterns (a lithography related effect). A maximum limit on the lateral motion of the junction at the surface, 0.5 micron, can be determined. The actual diffusion was less.

2.6 BIPOLAR TRANSISTORS

Bipolar transistors were fabricated by combining thermal and pulse annealing techniques. The objective was to demonstrate adequate control of junction depth with a high fluence, melting, pulse anneal in a geometry where two implants overlap (Figure 11).

The process sequence was: (1) growth of a 0.6 micron thermal oxide on an n-type wafer, then etch a region for implanting the base, 80 keV $3x10^{12}$ $^{11}B^+/cm^2$, (2) 0.2 micron of spin-on oxide was deposited and densified at 800°C, which annealed the boron implant, (3) an opening (100 micron o.d.) was then etched for the emitter implant of 30 keV, $3x10^{15}$ $^{75}As^+/cm^2$ which was covered with photoresist when a second (100 micron) opening was made for the contact to the base, 40 keV $2x10^{14}$ $^{11}B^+/cm^2$. After these steps the wafers were cleaned and given one of the following anneal cycles:

- 550°C 1 hr, PEBA at 1 J/cm^2, 550°C 1 hr
- 550°C 1 hr, PEBA at 1.2 J/cm^2, 550°C 1 hr
- PEBA at 1 J/cm^2, 550°C 1 hr
- PEBA at 1.2 J/cm^2, 550°C 1 hr
- 550°C 1 hr, 950°C 15 min

Contacts were applied, sintered at low temperature, and five devices from each type of anneal were tested.

The test results are shown in Figure 12. The prepulse anneal did not work out well in this test, and the low fluence pulse was not sufficient to anneal the devices. Apparently this fluence was very close to the threshold for annealing these implants. The I-V curves for the thermal (950°C) and high fluence PEBA devices are shown in Figure 12. The gain of both devices is approximately 40 at high current; the cause of the difference at low base current is not known.

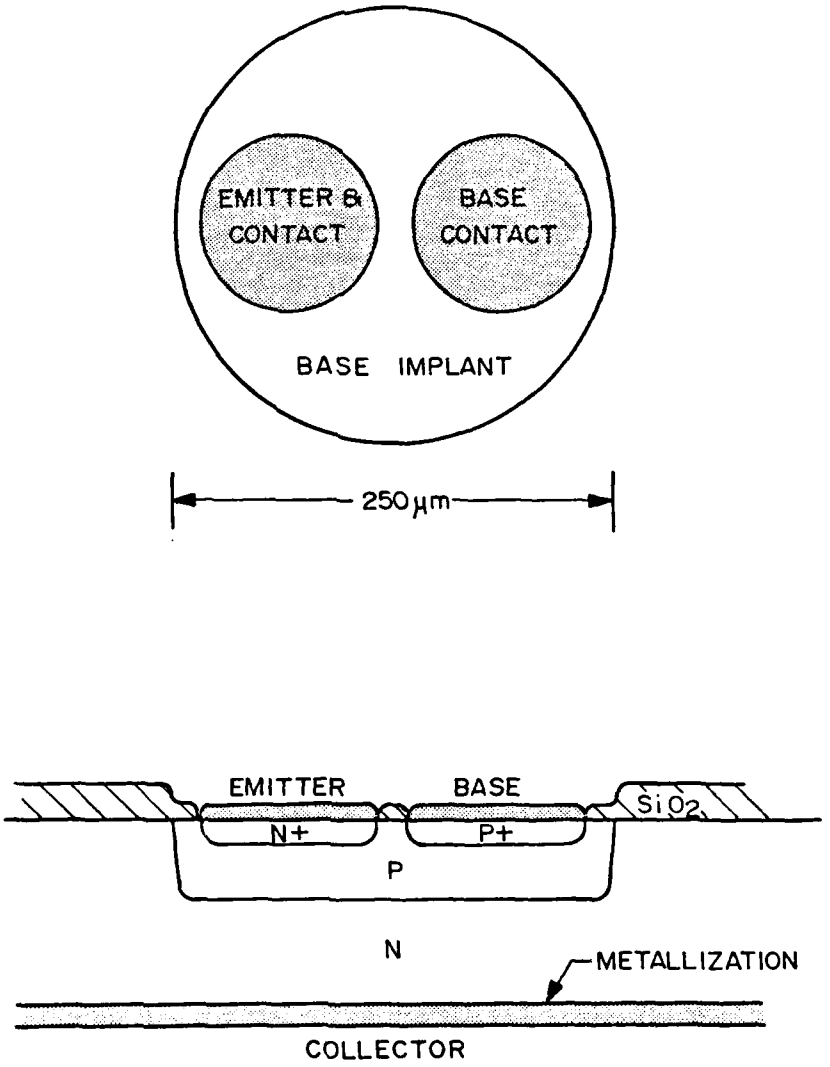


Figure 11. Bipolar transistor structure used to test PEBA process with overlapping junctions.

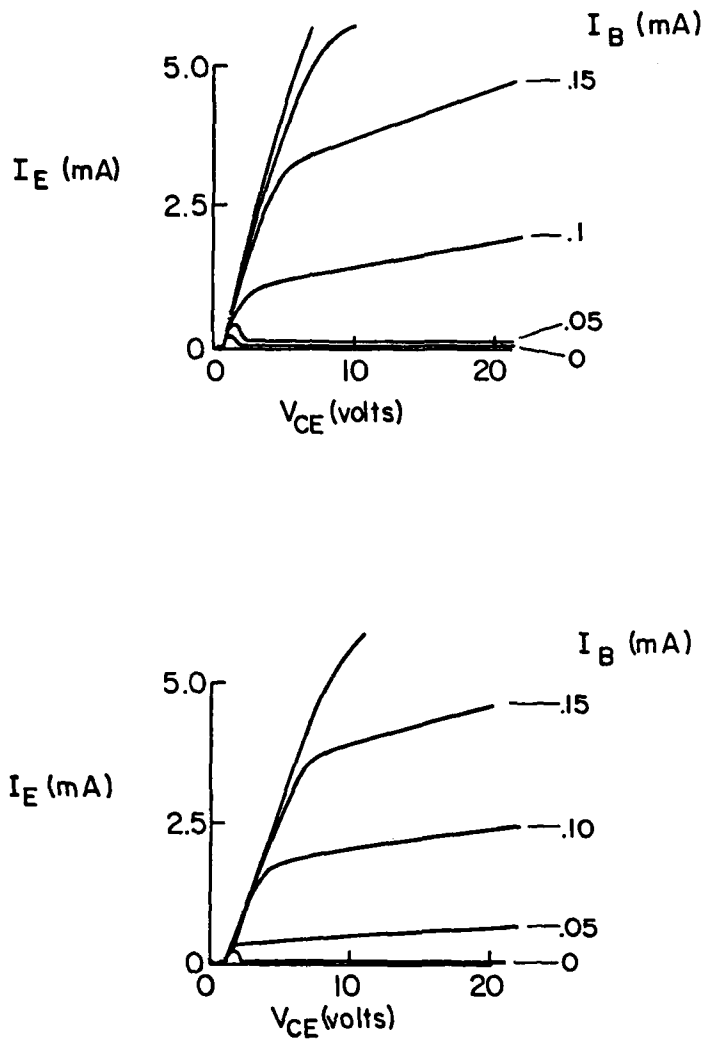


Figure 12. Characteristic I-V curves for npn bipolar transistors comparing PEBA and thermal anneal. (Note equal gain of 40.)

SECTION 3
FUTURE PLANS

3.1 OBJECTIVES

The remaining technical objectives for this program, as outlined in a technical review meeting with the contract monitor, Dr. R. Reynolds, are:

- Analyze pulse annealed diodes by DLTS.
- Fabricate a device with more than 2 leads by PEBA.
- Determine the uniformity of PEBA on a 1-2 micron scale.
- Determine the lateral diffusion of a junction under an oxide film edge.
- Establish solid phase annealing limitations.

These objectives are addressed by the six experiments, now in process, described in the following sections.

3.2 DELAY LINE TRANSIENT SPECTROSCOPY (DLTS)

DLTS can identify trap levels and concentrations in silicon in the region below a junction.[9] The depth sampled is variable and depends upon the doping level of the substrate, with typical values given in Table 6.[10] The junction can be a Schottky-barrier metal contact, or an implanted or diffused p-n junction.

The experiment in process will use n on p-type substrate diodes, fabricated by ion implantation of 2×10^{15} $^{31}P^{+}/cm^{2}$ at 10 keV and annealed by a pulsed electron beam. The structure, shown in Figure 13, is a modification of the JFET design, Figure 14, using that mask set to form a guard ring. Two types of substrates, 4 and 10 ohm-cm, will be used. Four different types of anneal cycles will be tested:

(1) PEBA

(2) PEBA and postpulse anneal

(3) PEBA of heated wafer

(4) None

TABLE 6. DEPTH ANALYZED BELOW JUNCTION BY DLTS

Carrier Concentration (cm^{-3})	Resistivity (ohm-cm)		Depth (microns)
	P-type	N-type	
2×10^{15}	10	4.0	0.8 - 2.0
2×10^{16}	1	0.5	0.25 - 0.8

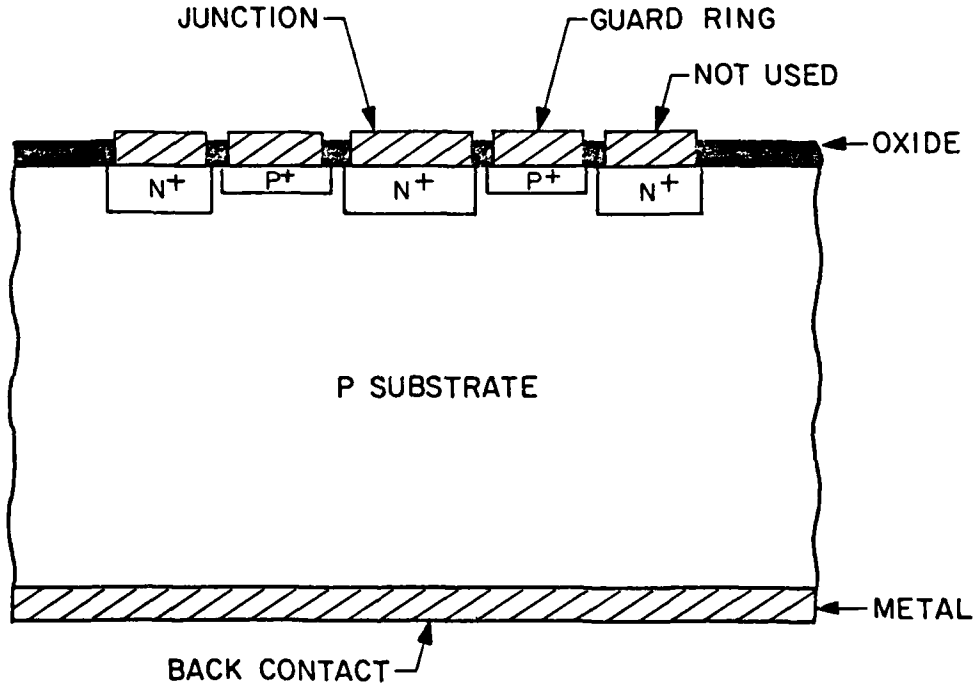


Figure 13. Structure for n^+ on p diodes to be used for DLTS measurements. Guard ring structure will use the JFET mask set (Figure 14) to reduce leakage currents. Contacts to the outer two rings are ungrounded and not used.

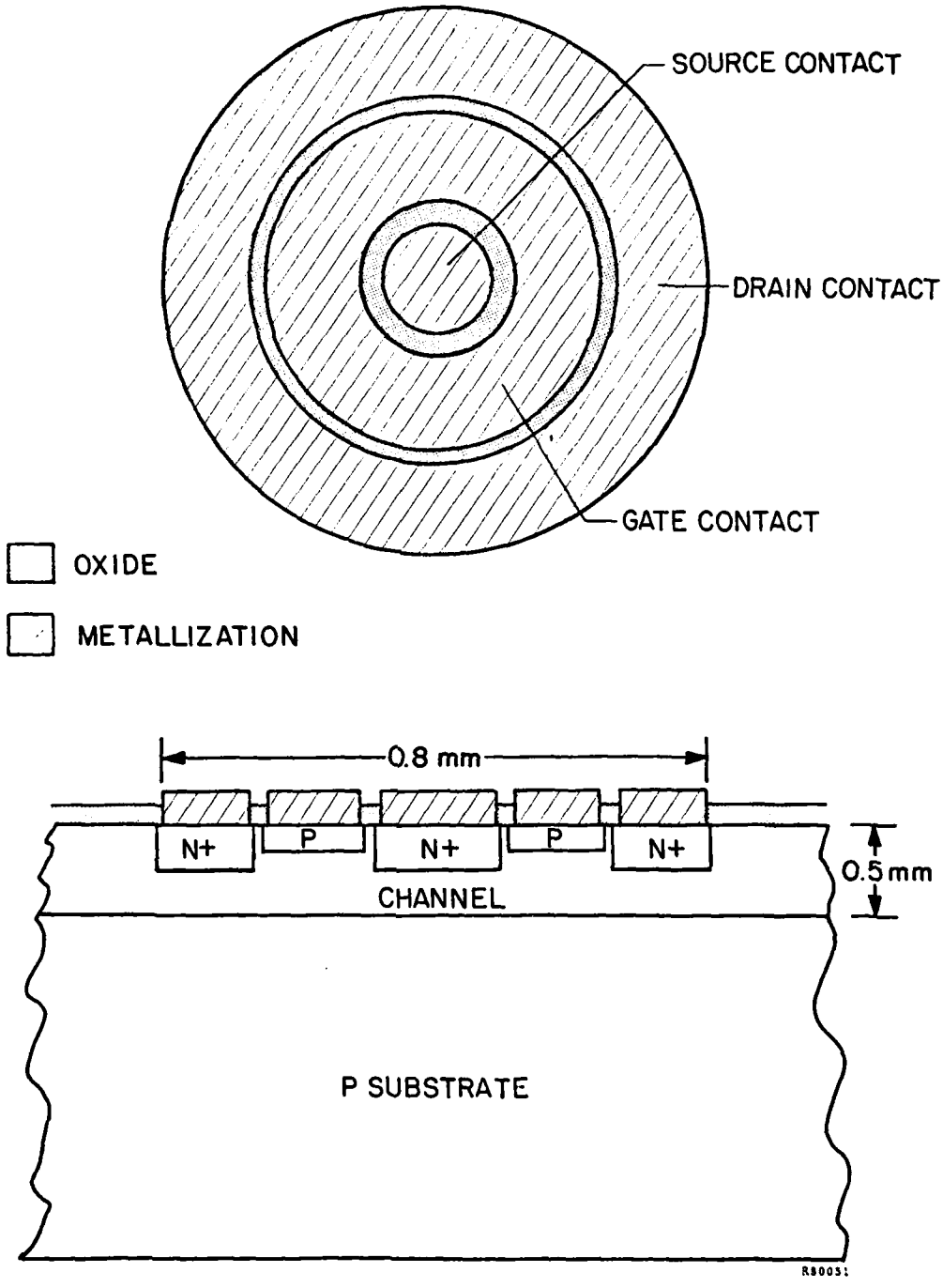


Figure 14. Ring-dot junction field effect transistor structure selected for testing PEBA and pulsed epitaxial regrowth for device processing.

The PEBA process will be a (presumed) melt phase anneal which has produced excellent solar cells from this type of junction. The post-PEBA anneal will be a thermal cycle at 400°C for 10 minutes in vacuum. This postpulse thermal cycle is the identical cycle used to heat wafers just prior to pulsing (Section 2.3). The no-anneal cycle is also an unimplanted wafer, furnished to Mr. H. DeAngelis[10] for analysis of the substrate without a pulse treatment. He will fashion Shottky barrier diodes in this material. Note that a PEBA diode (solar cell) with pulsed anneal was previously analyzed.[11]

3.3 JUNCTION FIELD EFFECT TRANSISTORS

Masks have been obtained for a ring-dot type of junction field effect transistor (JFET) (Figure 14). Since we are constrained by temperature limitations from using a thermal oxide for passivation, this structure, which will minimize surface effects, was chosen. This device will be used to test and evaluate the layers formed by the PEBLE process and PEBA ion implantation process, as well as to evaluate PEBA annealing of source, drain, and gate implantations. The source and drain can be either ion implanted boron (p) or a Schottky barrier junction. Initially these FETs will be fabricated using conventional CVD epitaxy to form the channel. The pulsed electron beam will be used to anneal the source and drain contacts and the gate junction. When this process is under control, devices will be made on wafers which have the channel layers formed by pulsed electron beam epitaxy or by pulsed electron beam annealed ion implantation. These devices will be electrically characterized and evaluated. This device was chosen as a viable test vehicle under this program, since junction field effect transistors, particularly enhancement mode Schottky FETs, are being seriously considered for use in VLSI circuits.

3.4 UNIFORMITY OF PEBA

An experiment has been planned to measure the uniformity of pulsed electron beam annealing on a 1-2 micron scale. Direct measurements of the fluence in the beam are not possible at this scale. Indirect measurements must be based upon some electrical property of the sample. The key parameter will be the junction depth. In the melting mode, the depth of melt is a sensitive function of the electron beam fluence (Figure 15). For complete annealing, the melt depth must extend to the maximum depth damaged by ion implantation. This will result in complete crystal regrowth and complete activation of the dopant.[12] Diffusion in the melt phase will alter the dopant profile[6] and cause the junction to be deeper than implanted. In the nonmelting model, field-enhanced diffusion[13] could also result in redistribution of the dopant and a deeper junction.

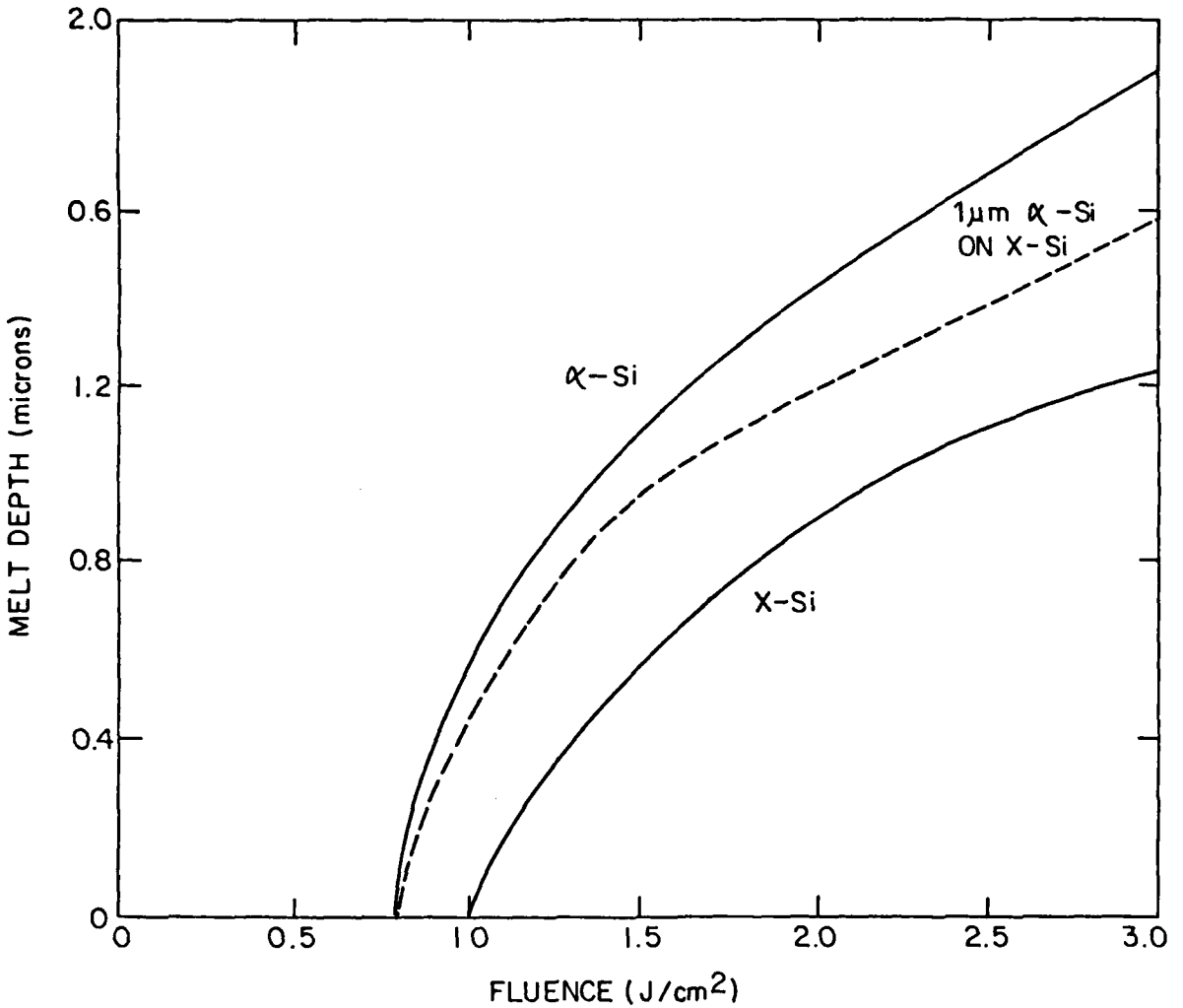


Figure 15. Melt depth in amorphous (α-Si) and crystal (x-Si) silicon as a function of pulsed electron beam fluence, other beam parameters described in reference 4. (Note choice of melting (1.0 J/cm^2) and non-melting (0.6 J/cm^2) fluence.)

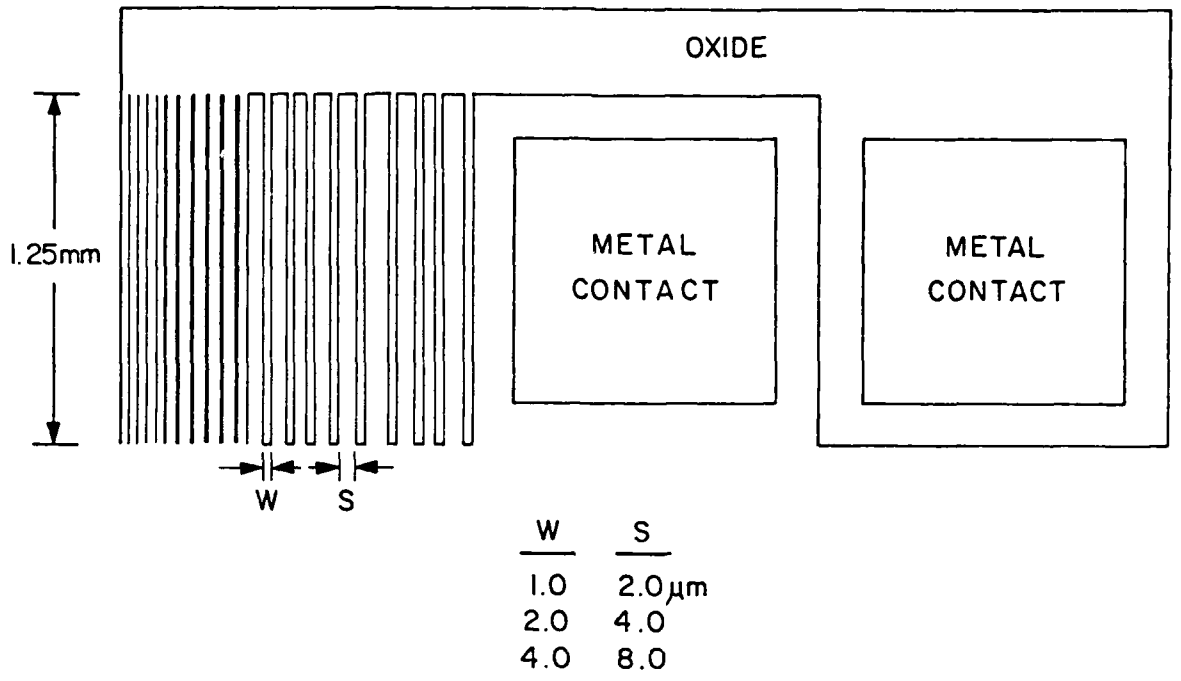
The measurement of uniformity, therefore, would be a measure of junction depth uniformity. Direct measurements by groove and staining showed no variation on a 10 micron lateral scale, although a small variation on a 1 mm lateral scale was seen. This measurement will be repeated. (Note that a 1 mm scale would correspond to the wire spacing in the anode mesh, a possible source of nonuniformity in the electron beam.) Measurements of the dopant profile by Rutherford backscattering with helium ions also showed little or no variation in depth with an analyzing beam of a few millimeters diameter. To improve upon the accuracy and resolution, a solar cell with a pulse annealed junction will be submitted for EBIC analysis (1-2 micron resolution). The experiment would compare furnace annealed ion-implanted junctions with PEBA, PEBA + postpulse anneal, and PEBA on a heated sample.

3.5 LATERAL DIFFUSION TEST

A new mask was made (Figure 16) for testing lateral diffusion. Measured line widths on the mask are 0.8, 1.5, and 3.0 microns. The lines are approximately 1.25 mm long. The design provides contacts to either the exposed or unexposed regions of the comb. Thus, with a back contact and a pulse annealed ion implanted junction, the mask can be used for an EBIC study of lateral diffusion. However, this is not expected to have sufficient resolution. A groove (or bevel) and stain is expected to show more accurately the position of the junction. With a submicron oxide line width, resolution to 0.1 micron may be possible with a stain that can be imaged in a SEM. An alternate technique, biasing the implanted region during SEM examination, will be tested to determine if the junction (at the surface) can be imaged directly. Resolution will generally be limited by lithography. Pre- and postpulse anneal comparisons are difficult due to contact application and removal.

3.6 SOLID PHASE ANNEALING

The proposed model of solid phase, fast pulse (0.1 microsecond) annealing is that the crystal structure of the sample is largely restored by a low temperature thermal anneal (550^{o}C) and that point defects and activation of the implanted dopant occur at high temperature during the pulse. The rationale behind the model is that rearrangement of a heavily damaged crystal structure about 0.1 micron deep takes several milliseconds[14] at near melt temperatures; but that a change in point defect structure



W	S
1.0	2.0μm
2.0	4.0
4.0	8.0

Figure 16. Test mask to measure lateral diffusion of junction during PEBA under submicron width oxide strips.

(e.g., an interstitial atom finds a substitutional lattice site) can be very fast at high temperatures while not occurring below some threshold. It is pointed out that melting or nonmelting cannot be definitely confirmed after processing if there is no change in surface morphology.

The anneal cycle, 550°C for 1 or 2 hours, followed by PEBA, was tested on a variety of boron implants. Increased activation of the dopant, by about a factor of 4, was observed, but comparisons to high temperature (950°C) anneals were not available. To determine more clearly what has happened, the series of experiments outlined in Table 7 will be performed. The principal diagnostic will be sheet resistance and junction depth measurements.

TABLE 7. MATRIX FOR SOLID PHASE ANNEAL EXPERIMENTS

Anneal Cycles	1.	550°C for 2 hours
	2.	550°C for 2 hours, 950° for 10 minutes
	3.	550°C for 2 hours, PEBA at 0.6 J/cm^2
	4.	550°C for 2 hours, PEBA at 0.6 J/cm^2, followed by 400°C 10 minutes
	5.	550°C for 2 hours, PEBA (hot) at 0.6 J/cm^2, T = 400°C during PEBA
	6.	Repeat No. 4, but double pulse
	7.	PEBA at 400°C at 1.2 J/cm^2
	8.	PEBA at 20°C at 1.2J/cm^2, then 400°C for 10 minutes ($^{31}p^+$ 10^{15}/cm^2)
Implants	1.	25 keV
	2.	50 keV
	3.	100 keV
	4.	200 keV
Total:	Over 32 variations are implied; some samples will be used for other tests. Substrates will be 1-2 ohm-cm, boron doped, (100), with a p^+/p back contact implanted and annealed prior to implanting the polished surface.	

3.7 HYDROGEN PLASMA ANNEAL

The pulse anneal process is known to produce some defects in the material below the junction region[15] which are attributed to fast quenching-in of defects. Most of these defects anneal out at 400°C (for 10 minutes) as reported here. Annealing in a hydrogen plasma at 200°C has been shown to be very effective as a postpulsed laser anneal[15]. Spire has arranged to process some 1 x 2 cm^2 solar cells comparing pulsed electron beam anneal and pulsed laser anneal with this postpulse thermal process.

SECTION 4
DISCUSSION AND CONCLUSIONS

During the past six months the effort on this contract was directed primarily at measuring the electrical characteristics of diodes, transistors, and resistors fabricated by ion implantation and pulsed electron beam annealing. Emphasis was placed on demonstrating effective annealing processes with the maximum temperature required in any thermal cycle limited to 550°C. Specific results are:

- Fabrication of low leakage current diodes by ion implantation and pulsed electron beam processing
- Demonstration that pulsed electron beam processing can be masked by thin oxide films with a geometric precision of at least 2 microns in line width
- Demonstration of a (probable) nonmelting anneal technique combining low temperature thermal and large area pulse techniques
- Fabrication of a bipolar transistor by ion implantation and PEBA
- Demonstration that pulse annealing a shallow, ion-implanted junction will not disturb a deeper, previously fabricated junction
- Determination that lateral diffusion of a junction during PEBA does not exceed 0.5 micron (and is probably much less)

Ongoing work will (1) refine the measurement of lateral diffusion during PEBA, (2) continue measurement of the electronic properties of pulse annealed material, and (3) fabricate a transistor (JFET) with all pulse annealed junctions.

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